SIEMENS

Semiconductor Group
Microcontrollers

Errata Sheet

June 16, 1998 / Release 1.4

Device: **C504-L / C504-2R**

Stepping Code / Marking: **AC**

Package: **MQFP-44**

This Errata Sheet describes the deviations from the current user documentation. The classification and numbering system is module oriented in a continual ascending sequence over several derivatives, as well already solved deviations are included. So gaps inside this enumeration could occur.

The current documentation is: Data Sheet 05.96
User's Manual 10.97
Instruction Set Manual 04.98

Note: ***Devices marked with EES- or ES are engineering samples which may not be completely tested in all functional and electrical characteristics, therefore they should be used for evaluation only.***

The specific test conditions for EES and ES are documented in a separate Status Sheet.

Change summary to last Errata Sheet Rel. 1.3:

- Minimum for supply voltage Vcc=4.75V at 40MHz clock frequency for all operating temperatures (for C504-L40/C504-2R40 only).

Functional Problems:

Problem 2: ROM verificatiion mode 1 is inoperable

The ROM verification mode 1 as described in the C504 User's Manual 06.96 on page 4-8 is inoperable. This means, that it's not possible to verify the internal ROM content using this specific ROM verification mode 1.

Workaround:

The internal ROM contents of C504-2RM parts are verified during device testing using another verification mode.

Problem 3: Timer 2 - Concurrent Access on T2CON

A problem might occur when Timer 2 is used together with the functionality of the P1.1/AN1/T2EX pin in the following operating modes :

- Timer 2 as baud rate generator
- Timer 2 in 16-bit capture
- Timer 2 in 16-bit auto-reload with DCEN=0

When a falling edge on P1.1/AN1/T2EX occurs during the execution of a read-modify-write instruction on SFR T2CON, the interrupt flag EXF2 is not set and and the related interrupt, if enabled, is not executed.

Workaround:

When using a read-modify-write instruction on T2CON, it must be checked (e.g. by software) whether a high-to-low signal transition occured at pin P1.1/AN1/T2EX during the execution of the read-modify-write instruction. This can be achieved by polling the level on P1.1/AN1/T2EX before and after the read-modify-write instruction. The timer 2 interrupt has to be disabled during the polling sequence. If a high-to-low signal transition is detected at P1.1/AN1/T2EX, the interrupt EXF2 flag can be set by software.

The following assembly program demonstrates a possible software workaround:

```
workaround:
        clr     et2             ; disable t2 interrupt
        jnb     p1.1, rmw1      ; normal rmw if pin is already low
rmw2:   orl     t2con, #xxh     ; rmw on t2con
        jnb     p1.1, force_t2int ; force t2int if p1.1 low now
        setb    et2             ; enable t2 int again
        sjmp    go_on           ; go_on, no falling p1.1-edge occured
force_t2int:
        setb    exf2            ; set request flag
        setb    et2             ; enable t2 int again, force interrupt exf2
        sjmp    go_on           ; go_on, falling edge occured within rmw
rmw1:   orl     t2con, #xxh     ; rmw on t2con
        setb    et2             ; ena t2 int again & go_on
go_on:
        ::::
```

Note :
If the external signal on P1.1/AN1/T2EX is a short pulse, the pulse width has to be 3 instruction cycles long at least. Otherwise the polling sequence of the pin cannot recognize the high-to-low signal transition.

Problem 4: Spike at CCx / COUTx pins

A write operation to SFR COINI will cause a spike from low to high level of about 10ns width (@ 20 MHz external microcontroller clock) at CCx or/and COUTx, if these pins are assigned to the CCU in the following way :

- CCx or/and COUTx pins are programmed as compare output of the CCU (corresponding bits in SFRs CMSEL0 or CMSEL1 set)
- The COINI register has a "0" in a CCx/COUTx pin related bit position
- Related CCx/COUTx pins are at low level during the write operation to SFR COINI

The occurence of the spike is independent of the state of compare timer 1 (running or stopped).

Workaround:

During initialization of the CCU, the spike can be avoided if COINI is written before CMSEL0 or CMSEL1 are written. If the CCU is running, COINI should be never written. If the write operation to COINI is absolutely required. While the CCU is running, an external low pass filter can be used e.g. to suppress the spike at the CCx / COUTx pins.

Deviation from Electrical- and Timing Specification:

Problem 1: ± 4 LSB total unadjusted error (TUE) of A/D converter

The total unadjusted error of the A/D converter does not meet the specified value of the DC characteristics. The value for TUE is limited as follows :

$$TUE = \pm 4 \text{ LSB} \quad \text{in the } V_{IN} \text{ range : } \quad V_{SS} < V_{IN} < V_{CC}$$

Problem 2: Minimum supply voltage Vcc=4.75V at 40 MHz clock frequency

The minimum rating for supply voltage at 40 MHz clock frequency is Vcc=4.75V for all operating temperatures (for C504-L40/C504-2R40 only).

History List (since last CPU Step AB)

Functional Problems

Functional Problem	Short Description	Fixed
1	Wrong destination address at AJMP and ACALL instructions	step AC
2	ROM verificatiion mode 1 is inoperable	-
3	Timer 2 - Concurrent Access on T2CON	-
4	Spike at CCx / COUTx pins	-

AC/DC Deviations

AC/DC Deviation	Short Description	Fixed
1	± 4 LSB total unadjusted error (TUE) of A/D converter	-
2	Minimum supply voltage Vcc=4.75V at 40 MHz clock frequency	-

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